CLAIMS

1. A logic circuit which comprises:

(a) a precharge node for retaining one of a high signal state and a relatively low signal;

(b) an input terminal;

(c) a first transistor of one of n-channel or p-channel type having a control electrode and a current path coupled between a source of power and said precharge terminal;

(d) a second transistor of the other of n-channel or p-channel type having a current path coupled between said input terminal and said control electrode of said first transistor and a control electrode; and

(e) circuitry coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node to control current flow in said current path of said second transistor.

2. The circuit of claim 1 further including a pair of transistors having serially connected current paths, said serially connected current paths being coupled between said precharge node and a reference source.

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3. The circuit of claim 1 wherein said circuitry coupled to said control electrode of said second transistor and responsive to the status of said precharge node includes an inverter having an input coupled to said precharge node and an output and a feedback circuit coupled between said output and said control electrode of said second transistor.

4. The circuit of claim 2 wherein said circuitry coupled to said control electrode of said second transistor and responsive to the status of said precharge node includes an inverter having an input coupled to said precharge node and an output and a feedback circuit coupled between said output and said control electrode of said second transistor.

5. The circuit of claim 1 wherein said circuitry coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node includes an inverter having an input coupled to said precharge node and an output and a feedback circuit coupled between said output and said control electrode of said second transistor.

6. The circuit of claim 4 wherein said circuitry coupled to said control electrode of said second transistor and responsive to one of said high signal and said low signal at said precharge node includes an inverter having an input coupled to said precharge node and an output and a feedback circuit coupled between said output and said control electrode of said second transistor.

7. The circuit of claim 6 further including a third transistor of said one of n-channel or p-channel type coupled between a source of power and said control electrode of said second transistor and responsive to a said low signal at said output terminal to maintain said first transistor in an inactivated state.

8. The circuit of claim 6 further including a fourth transistor of said one of n-channel or p-channel type coupled between a source of power and said precharge node and responsive to said low signal at said output terminal to maintain said precharge node at said high signal state.

9. The circuit of claim 7 further including a fourth transistor of said one of n-channel or p-channel type coupled between a source of power and said precharge node and responsive to said low signal at said output terminal to maintain said precharge node at said high signal state.

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10. The circuit of claim 2 wherein the control electrode of one of said pair of transistors is coupled to said control electrode of said second transistor.

11. The circuit of claim 7 wherein the control electrode of one of said pair of transistors is coupled to said control electrode of said second transistor.

12. The circuit of claim 10 further including a fifth transistor of said one of n-channel or p-channel type having a current path in parallel with said second transistor and a control electrode couple to said precharge node.

13. The circuit of claim 11 further including a fifth transistor of said one of n-channel or p-channel type having a current path in parallel with said second transistor and a control electrode couple to said precharge node.

14. The circuit of claim 4 wherein the control electrode of one of said pair of transistors is coupled to a portion of a current path to said second transistor remote from said first transistor and further including a second inverter coupled to transmit current therethrough from said output of said inverter to said precharge node.

15. A domino logic circuit which comprises:

(a) an input terminal;

(b) a precharge node;

(c) a first switch responsive to a second switch sensing one of a high or low voltage at said precharge node to charge said precharge node; and

(d) said second switch responsive to said one of a high or low voltage at said precharge node to control said first switch charging said precharge node.

16. The circuit of claim 15 wherein said first switch is a p-channel transistor and said second switch is an n-channel transistor.

17. The circuit of claim 15 further including an output terminal, an inverter coupled between said precharge node and said output terminal and feedback circuitry coupled between said output terminal and coupled to said second switch to provide said charge state of said precharge node to said second switch.

18. The circuit of claim 16 further including an output terminal, an inverter coupled between said precharge node and said output terminal and feedback circuitry coupled between said output terminal and coupled to said second switch to provide said charge state of said precharge node to said second switch.

19. The circuit of claim 15 further including a pair of transistors having serially connected current paths, said serially connected current paths being coupled between said precharge node and a reference source.

20. The circuit of claim 18 further including a pair of transistors having serially connected current paths, said serially connected current paths being coupled between said precharge node and a reference source.

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